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DC offset removal of thyristor switched series capacitor and in a novel and simple method

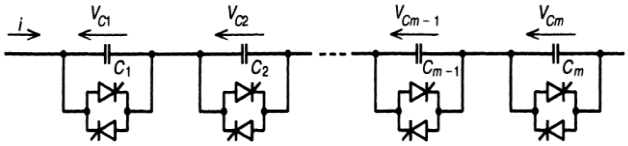
M Mahdi Mansouri[1], Majid Nayeripour[2]
[1] Yazd Regional Electric Co, Iran
[2] Shiraz University of Technology, Shiraz, Iran

Abstract
As a DC offset is produced when each step of Thyristor Switched Series Capacitor (TSSC) come in and out operation, this DC offset is analyzed and effective parameters are discussed. Then a simple method for its elimination is proposed.
The first result of proposed method is that DC offset is removed in half cycle. Another advantage of proposed method is that delay time of TSSC steps for outage reduces from one cycle to half cycle. It means that operation response of TSSC is improved. The proposed method can be used in other series compensators with multi steps.

Keywords: thyristor switched series capacitor, dc offset, speed increasing of thyristor switched series capacitor

1. Introduction
Thyristor Switched Series Capacitor (TSSC) in one of the Flexible Alternative Current Transmission System (FACTS) equipments which are used for line series compensation, transmission line capacity increase and improvement of voltage stability margin increase [1, 5, 6, 13, 15]. There are a few researches on this compensator because of its simplicity. This compensator has some advantages like low harmonic production, simple control, using low voltage switches. Whereas this compensator has capabilities like stability improvement, power oscillation damping, and capacity increasing of line transmissions. TSSC has response time equal to one cycle delay like other compensators [5, 13].
TSSC has some difference with other series compensators for example, TSSC has discontinuous impedance unlike TCSC that has continuous impedance or unlike SSSC that has variable voltage equivalent circuit. But TSSC have similar manner with increasing its step and decreasing its step values [1-4, 6, 13].
When a series capacitor is entered in transmission line, a DC offset will be created in the voltage. This voltage can cause some problems like core saturation of power transformers and metering transformers. Outage of a series capacitor can also increase DC components of fault current. This effect will increase mal operation of protection relays [1, 7-10, 13, 17].
This DC offset can be created in other series compensators like TCSC [11-13, 16], although this problem has not been noticed yet.
The operation and advantage of TSSC is discussed at the first and creation of DC voltage will be shown, Then DC voltage offset is analyzed and its main parameters are discussed in details for the first time.
A simple and effective method is proposed for elimination of DC offset component. A circuit is simulated for evaluation the proposed method. Another advantage of proposed method is that TSSC response increases in capacitor bank outages.

2. TSSC Analysis
TSSC contains some series capacitor and two anti-parallel thyristor for each of them as shown in Figure 1). The compensation base of TSSC is bringing in and out of this capacitor steps in operation. Different percentage of series compensation is produced with combination of these capacitor inductances.



TSSC configuration [1]
TSSC has these advantages
- -Using thyristors is caused that different steps can come in and out for unlimited times at maximum one cycle delay in comparison with mechanical switches [1].
- TSSC can increase or decrease the line capacity in one cycle. This time is enough for some application like power oscillation damping [5].
- TSSC has simple switching and control in comparison with Thyristor Controlled Series Capacitor (TCSC) [1].
- TCSC has a inhibited area that it makes possibility of instability of grid but TSSC does not have this behavior [6].
- TCSC has series compensation between minimum series compensation impedance ($X_{se}^{\min}$) and maximum series compensation impedance ($X_{se}^{\max}$) and it does not have series compensation near the zero ($X_{se}^{\min} = 0$) [1].
- TSSC does not create harmonics [1].

A.DC Offset
As, the thyristors turn off in zero current in natural

commutation and turn on always in zero current, two anti-parallel thyristors are always ON and they will turn off when a decision is made for coming in a capacitor step. The thyristors will turn off in the first zero current after turning off command and the capacitor back put in series with line.
As thyristors turns on in zero current and capacitor has zero initial voltage, the capacitor voltage reaches to its maximum in half cycle and it creates a DC offset in voltage [1].
If transmission line is considered as current source, a DC voltage offset will be created as shown in Figure 2) [1, 14]. This subject is clearer in TSSC because of its pure switching. This offset can cause core saturation of power transformers and metering transformer and error in protection systems [1, 7-10, 17].

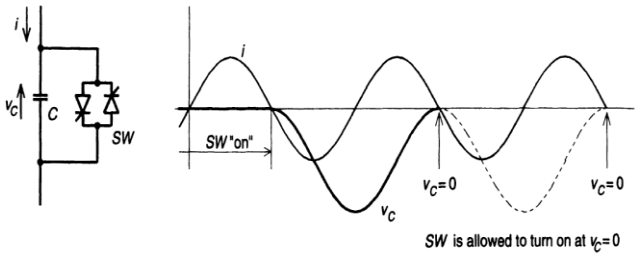


Fig 2: DC voltage offset of TSSC [1]

Thyristors must turn on for capacitor outages and capacitor bypassing. This action must be done in capacitor zero voltage for stress reduction of thyristors. As shown in Figure 2), the turning off condition will have one half cycles more delay because of DC offset existence [1].
In ideal condition, the DC offset component is equal to capacitor maximum voltage (V_C^{Peak}). The capacitor maximum voltage depends on capacitor capacity and line current as (1):

$$V_C^{Peak} = I_{Line}^{Peak} \cdot X_C \tag{1}$$

As series compensation is done in transmission line with heavy current, this DC offset will be considerable. The DC offset depends on capacitor capacity also. The series compensation usually is about 60% of line reactance. This impedance is divided to some steps in TSSC. Therefore, the steps capacity is relatively small. The impedance characteristic of a 400kV, 600km, 50Hz transmission line with $l = 1mH/km, c = 11.1\times10^{-9} F/km$ is equal to (2):

$$Z_n = \sqrt{\frac{l}{c}} = \sqrt{\frac{10^6}{11.1}} = 300\Omega \tag{2}$$

$$\beta = \omega\sqrt{lc} = 0.06^\circ / km$$
$$\theta = 36^o \tag{3}$$

$$P_{\max} = \frac{P_n}{Sin\theta} = 907.4MW \tag{4}$$

The capacitor reactance for series compensation is obtained as [1]:

$$k_{se} = \frac{X_c}{2Z_n} Cot\frac{\theta}{2} \tag{5}$$

If percentage of series compensation is considered as $k_{se} = 0.5$ and number of capacitor banks is considered as n=10 then each step reactance will be:

$$X_c = \frac{1}{n} 2k_{se} Z_n \tan\frac{\theta}{2} = 0.1\times300\times\tan18^\circ = 9.748\Omega \tag{6}$$

Therefore, the DC offset will be smaller for increasing of capacitor steps number.

b. Effect of DC offset on bus voltages of grid

The bus voltages of grid before DC offset and series compensation are:

$$V_2\angle\delta = V_1\angle0 + jX_L I_{line}\angle\phi$$
$$V_2\angle\delta = V_1\angle0 + X_L \cdot I_{line}\angle\phi + 90 \tag{7}$$

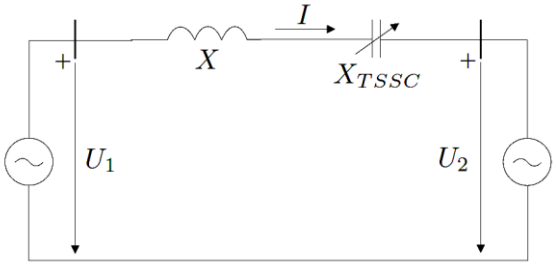


Fig 3: After compensation

And after series compensation as shown in Figure 3):

$$V_2'\angle\delta' = V_2\angle\delta + jX_C I_{line}\angle\phi$$
$$V_2'\angle\delta' = V_1\angle0 + (X_L - X_C)\cdot I_{line}\angle\phi + 90 \tag{8}$$

Therefore, the end voltage of transmission line will have DC offset with assumption of constant line current because of $V_2'\angle\delta' = V_2\angle\delta + V_C$.

c. Effect of DC offset on line current

If the sending and receiving end voltage of a transmission line is assumed constant, the line current before compensation is

$$I_{line}\angle\varphi = \frac{V_1\angle0 - V_2\angle\delta}{jX_{line}} \tag{9}$$

And if DC offset is not considered, the line current after compensation will be:

$$I'_{line}\angle\varphi = \frac{V_1\angle0 - V_2\angle\delta}{j(X_{line} - X_C)} \tag{10}$$

Equation (10) shows that amplitude of line current is changed without angle changing. But if DC offset is considered, the line current will be[8-10]:

$$I'_{line}\angle\varphi = \frac{V_1\angle 0 - V_2\angle\delta - V_{DC}}{j(X_{line} - X_C)} \quad (11)$$

This means that there is a DC component in line currents. This value is:

$$I_{DC} = \frac{-V_{DC}}{j(X_{line} - X_C)} = \frac{-jX_C I_{line}}{j(X_{line} - X_C)}$$

$$I_{DC} = \frac{\frac{k_{se}}{n}}{1-\frac{k_{se}}{n}} I_{line} \quad (12)$$

Therefore, the other lines and buses will have DC offset.

d. The proposed method for DC offset elimination

As the DC offset is produced in direction of the first current injection cycle to capacitor, the idea is that two capacitor step must come in series with a half cycle delay between them. Therefore, the DC offset that is created by first capacitor step, will be canceled by the second step in opposite phase.

The similar procedure must do for DC offset elimination in outage of capacitor steps.

Simulation

A TSSC with two capacitor bank is simulated in Matlab/Simulink as shown in Figure 4).

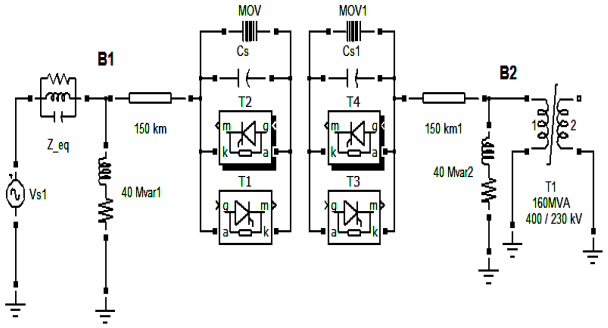


Fig 4: A TSSC with two capacitor bank

The DC offset, the sending and receiving end voltage of transmission line is shown in Figure 5). The first capacitor is come at 0.305second.

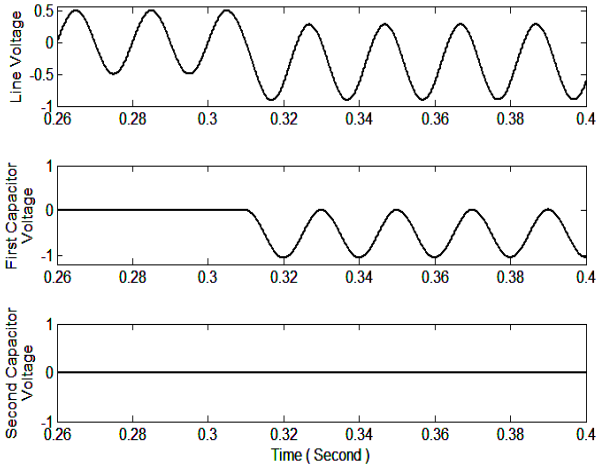


Fig 5: The first step capacitor coming and creating DC offset

A DC offset is created when the first capacitor step is brought series in line. This DC component will damp in long time depending to grid parameters. This time is 30 second for simulated circuit as shown in Figure 6). This time and this component can be dangerous for power system.

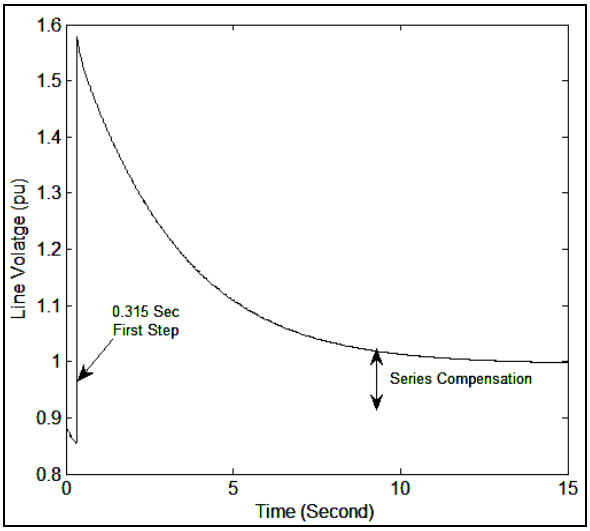


Fig 6: Damping of DC offset in 30 seconds

If the second step is brought to service base on the proposed method, the DC offset will eliminate as shown in Figure 7) at 0.315 seconds (in half cycle).

As the DC offset amplitude depends on capacitor impedance

and line current, entrance of each step of TSSC will change the working point of grid. This effect is not considered in the simulations of this paper.

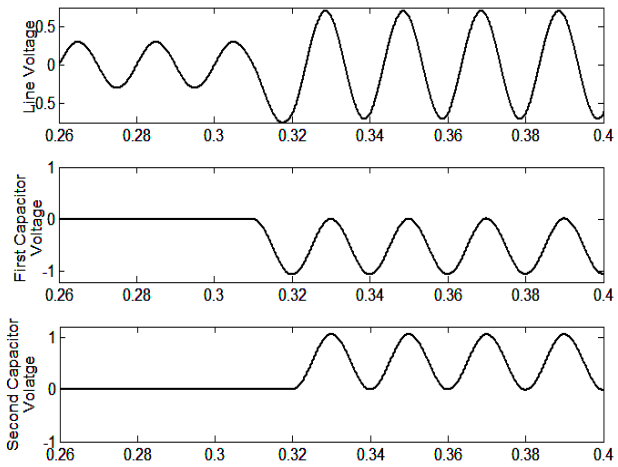


Fig 7: DC offset elimination after half cycle

A. Outage time reduction

If compensator wants to out one step as fast as possible, and if DC offset is existed, the one step outage will be delayed to the first zero crossing and it will have one cycle delay at maximum as shown in figure 5).

But if DC offset is eliminated, the thyristors can bypass the capacitor in first zero crossing that it will have half cycle delay at maximum. This advantage makes TSSC faster. This advantage brings better power oscillation damping and stability improvements for TSSC.

B. DC offset in step Outages

Similar offset can be created in outage of each capacitor step. The DC offset can be canceled in similar way. The second step outage after each capacitor outage will eliminate the DC offset in half cycle.

Conclusion

A DC voltage offset is created in each TSSC steps. A simple and effective method is proposed in this paper for elimination of this DC offset in half cycle. This method also reduces the TSSC response time to steps outage from one cycle delay to half cycle.

As the DC offset amplitude depends on capacitor impedance and line current, entrance of each step of TSSC will change the working point of grid. Increasing the number of steps will decrease the size of each step; therefore DC offset will be small in comparison with nominal voltage of grid. In any way this method reduces the DC offset damping time from multi ten seconds to a half cycle.

The proposed method can do for other series compensators that have more than one step. The proposed method can be used for power oscillation damping and fault detection in series compensated line in future studies.

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