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Electrical and structural evaluation of different MOSFET designs

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Abstract

The cornerstone of the electronics industry is the invention of the transistor. Nano electronics technology has advanced thanks in large part to Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). In this study, some of the most widely used MOSFET structure designs are briefly reviewed. Because to short channel effects and DIBL, the Moore's Law-proposed scaling down of planar bulk MOSFETs has reached saturation. Alternative methods to address the issues at lower node technologies have been contemplated as a result. Two interesting options in this field are SOI and FinFET technology.

Keywords: Mosfet, transistor, scaling, gate length, semiconductor

Introduction

Since their creation in the 1960s, Metal Oxide Semiconductor Field Effect Transistors, or MOSFETs, have revolutionized the semiconductor industry. Despite being slower than a bipolar junction transistor, a MOSFET can accommodate more transistors since it is smaller, less expensive, and consumes less power. The two main characteristics of a transistor are its gate width (W) and length (L). The distance an electron must travel from a highly doped source to a drain is known as the gate length. The gate length is referred to as X-nm. About "0.7 times the previous technology" is what each lower node technology is, such as 130 nm, 90 nm, 65 nm, 45 nm, and so on. According to the International Technology Roadmap for Semiconductors (ITRS), the 22 nanometer (22 nm) is the next CMOS process step after the 32 nm level. Each node has a factor of 0.7 for transistor length, breadth, and oxide thickness. While gate capacitance decreases by a factor of 0.7 with scaling, transistor channel resistance remains constant. Consequently, the transistor's RC delay scales with a factor of 0.7. Every year, the processors get 17% quicker and use less power.

For a number of reasons, smaller MOSFETs are required. Transistors are being made smaller primarily to accommodate an increasing number of devices in a particular chip space. As a result, there may be chips with greater functionality in the same space or chips with comparable capability in a relatively small area. Since a semiconductor wafer's manufacture costs are mostly constant, the cost per integrated circuit is mostly determined by how many chips can be made on a single wafer. Therefore, a smaller IC size allows for the production of more chips per wafer, which lowers the cost per chip.

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Bulk Planar Mosfet

Over the past 40 years, the semiconductor industry's mainstay has been the planar bulk-silicon MOSFET. However, by 2009, gate lengths below around 32 nm (sub-45 nm half-pitch technology node) would make it more challenging to scale bulk MOSFETs. Short-channel effects (SCE) are much reduced as the gate length is reduced because of an increase in the capacitive coupling of the channel potential to the source and drain in relation to the gate. This shows up as:

a. A rise in off-state leaks
b. Roll-off of the threshold voltage (VTH), which results in a lower VTH for shorter gate lengths.
c. Rain-induced barrier lowering (DIBL), a decrease in VTH as drain bias increases because the drain voltage modulates the source-channel potential barrier.
d. Swing below the threshold

All of these technologies are currently getting close to critical physical constraints, which might prevent future device size expansion.

A MOSFET is schematically shown by two back-to-back coupled p-n junctions in Figure 2.1. A metal-oxide semiconductor (MOS) capacitor's carrier density is controlled by the gate voltage that is put across it, which also forms an inversion channel between the source and the drain. The MOSFET's gate length and gate dielectric thickness are two crucial structural factors from an operating perspective. Both the vertical and lateral dimensions of the device are impacted by MOSFET scaling. While a chip's transistor density rises as its lateral dimensions are reduced, effective electrostatic integrity requires a drop-in oxide thickness.

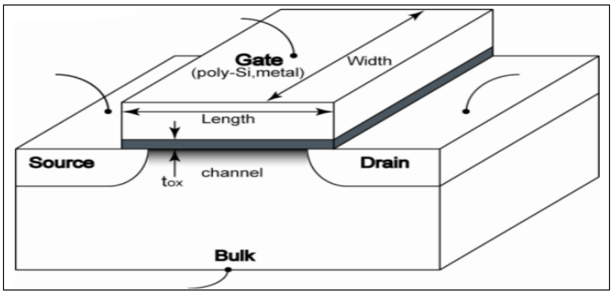

Fig 1: Schematic View of a Surface-Channel

Physical gate length, channel width, and physical gate dielectric oxide thickness (tox) are shown by the MOSFET device.

The drain current Id in modern MOSFETs is established by:

$$\frac{I_d}{W} = C_{ox}(V_G - V_{th})v \qquad (1)$$

where v is the source end carrier velocity, Cox is the gate capacitance per unit area, and W is the channel width. It is possible to determine the saturation transconductance gm by:

$$\frac{g_m}{W} = \frac{\partial I_d}{\partial V_g} / W = C_{ox} \text{ x } v = \frac{\varepsilon_{ox}}{t_{ox}} \text{ x } v \qquad (2)$$

where the oxide permittivity is denoted by ox. At short-channel MOSFETs, the carrier velocity is typically saturated, hence gm/W serves as an indicator of gate oxide thickness tox. Both the device current and the saturation transconductance are strongly correlated with oxide thickness because gate capacitance per unit area is inversely proportional to oxide thickness.

To maintain the proper gate voltage overdrive in accordance with equation (1), the threshold voltage has also been lowered. However, the scaling of gate length and gate dielectric thickness has not kept pace with the decrease in supply voltage and threshold voltage. Increasing channel doping required to manage shortchannel effects is one of the factors contributing to the slower threshold voltage lowering. In turn, the sublinear threshold voltage scaling has delayed the supply voltage's scaling.

Since scaling started, the MOSFET substrate doping—and particularly the channel doping concentration—has been steadily rising. In modern 35 nm gate length MOSFETs, the doping density has already surpassed 2×1018 cm-3, up from the initial value of around 2.5×1016 cm-3 in 1 µm gate length transistors [2].

The gate dielectric thickness in MOS devices has been the most aggressively expanded and is the single most crucial device parameter to allow device growth. A thin gate dielectric lessens the source/drain impact on the channel by increasing the capacitive coupling between the gate and the channel. Increased ON-state drive current, or a bigger inversion charge density, is also a result of a larger gate capacitance.

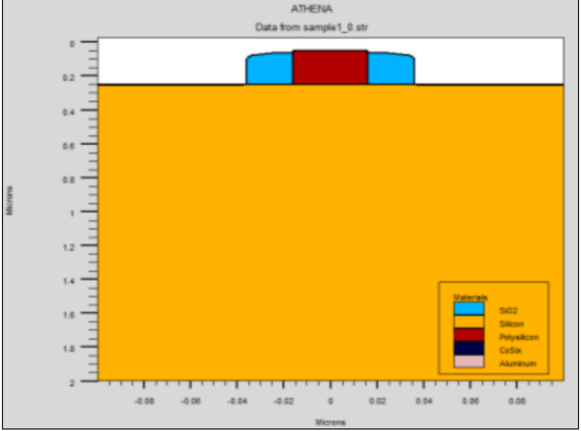

Fig 2: Planar Mosfet

The following are some ways that scaling down has an impact:

1. Reduced subthreshold swing;
2. VT decrease with increasing drain voltage (drain induced barrier lowering, or DIBL);
3. Decline of threshold voltage with attenuation of gate length (VT roll-off).

These occurrences are collectively referred to as "short channel effects" (SCE), and they have a tendency to raise the off-state static leakage power.

SOI MOSFET

Instead of using traditional silicon substrates, silicon on insulator (SOI) technology use a stacked silicon-insulator-silicon substrate to lower parasitic device capacitance and enhance circuit performance [3].

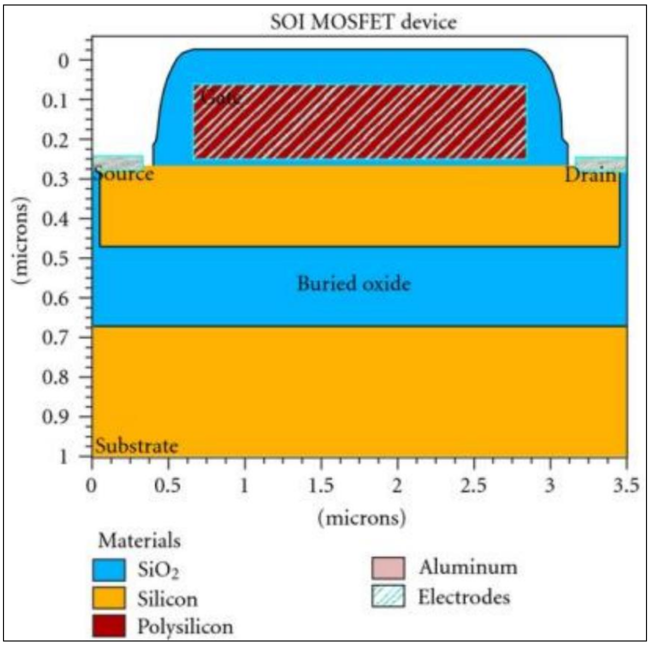

Fig 3: SOI MOSFET

Fully depleted and partially depleted SOI MOSFETs are the two varieties of SOI MOSFET. Because of the extremely thin silicon layer on top of the totally depleted SOI MOSFETs, the channel is entirely drained of the majority of carriers, hence the term "fully depleted." As a result, the SOI layer is very thin in relation to the device's depletion width. As a result, the gate can efficiently regulate the voltage.

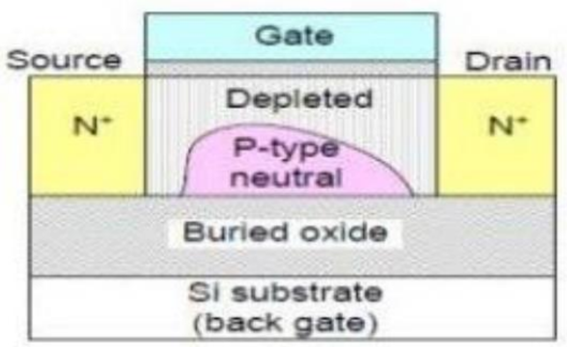

Fig 4: Partially Depleted SOI MOSFET

Consequently, the MOSFET's body lacks a neutral area that is capable of receiving a charge. Better short channel performance and the removal of the floating-body phenomenon are two benefits of FD SOI MOSFETs.

The SOI layer thickness for a partially depleted SOI MOSFET is more than the gate's maximum depletion width. The thickness of the silicon layer is often greater than 50 nm, which enhances the device's threshold voltage and sensitivity constraints. Compared to conventional planar bulk CMOS, PD SOI MOSFET architectures are simpler to build and have a lot more suitable process and device design. PD SOI devices are generally best suited for high-speed applications that require the greatest clock rates. However, the floating body effect is the main problem with the half-exhausted gadget.

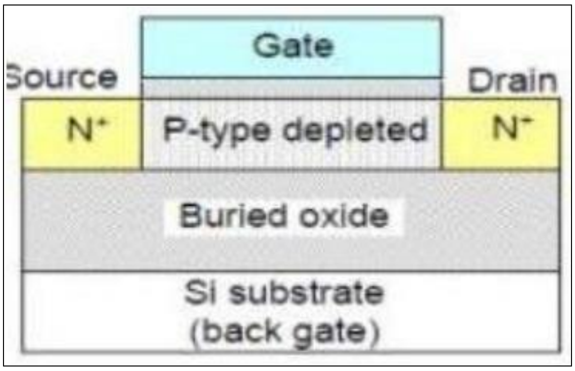

Fig 5: Fully Depleted SOI MOSFET

Compared to PD SOI MOSFET, FDSOI MOSFET has a smaller leakage current. The threshold voltage, gate oxide thickness, and channel length all have an inverse relationship with the leakage current. PD SOI MOSFETs have a higher threshold voltage than FDSOI MOSFETs. Kink effect, the primary disadvantage of PDSOI MOSFET, is removed in FDSOI MOSFET [4].

Multi Gate MOSFET

Out of all the multi-gate MOSFET architectures, the FinFET design shows the most promise. A thin silicon body called a fin and gate terminal are wrapped around this structure. Because of its many gates and ease of fabrication, FinFET has been deemed by ITRS to be the most significant substitute for planar MOSFETs.

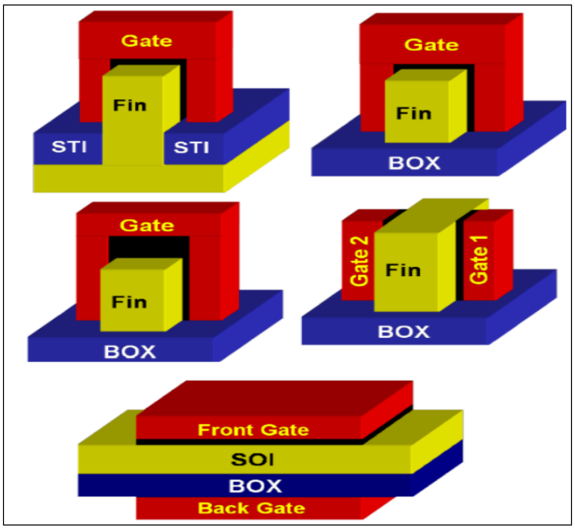

Fig 6: Various Structures of Multi Gate MOSFET Devices

This device can produce BULK FinFETs or SOI FinFETs depending on whether it is constructed over a bulk or SOI substrate. Double gate FinFET is created if the oxide hard mask on top of the fin is left in place. The top surface of the fin in this design does not conduct current; with triple gate FinFETs, however, both the top surface and the sides do. Two independently biased gates can likewise be used to create a FinFET. This may be accomplished by employing the chemical mechanical polishing process to erase the top part of a standard FinFET's gate, creating an independent double gate [5].

Conclusions

All of the MOSFET designs that are now available have been briefly reviewed in this publication. Multi-gate MOSFETs are superior than traditional planar schemes, according to an analysis of the structures of all the designs mentioned above. Additionally, the scaling down of transistors due to SOI technology has revolutionized the ability to pack more in the same amount of space. Another promising development in this sector is FinFET technology.

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